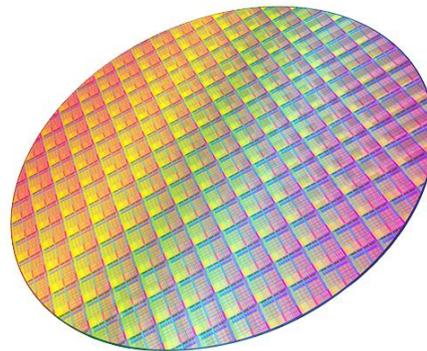


ANSYS SEMICONDUCTORS Update in 2020 R1

To meet the growing demand for increased signoff coverage for next-generation, ultra-large and high-performance system-on-chips (SoCs) driving AI, 5G and automotive applications, ANSYS' semiconductor portfolio of power and reliability solutions has been enhanced to drastically improve scenario coverage and accelerate time to results.



ANSYS PowerArtist features static power efficiency checks that serve as early signoff criteria to qualify RTL IP without requiring vectors and accelerates time-to-power for emulator-generated long activity scenarios. ANSYS RedHawk-SC's novel no-propagation vectorless (NPV) dynamic analysis approach efficiently identifies power grid weakness in the absence of simulation vectors and enables a more than 90% switching coverage. ANSYS Totem's new adaptive meshing algorithm supports large PMIC designs with a 4X–5X runtime improvement and a 20–40% memory footprint compared to traditional FEM solutions, while providing silicon-correlated accuracy.

The Totem and RedHawk product family is also certified for a comprehensive list of FinFET nodes down to 4nm/3nm process technology and 2.5D/3D-IC packaging technologies for multiphysics signoff across major foundries.

The new era of semiconductors will enable transformational products for artificial intelligence (AI), 5G, automotive, networking, cloud and edge compute applications. Ubiquitous connectivity, low latency and faster data rates will enable billions of more smart devices. These devices will rely on advanced, low power FinFET designs and state-of-the-art 3D integrated

circuit (IC) packaging technologies to deliver the required power, performance, area and reliability metrics.

Multiphysics analysis is critical for enabling these cutting-edge electronics systems to work reliably throughout their lifetime. ANSYS empowers customers with multiphysics simulations to simultaneously solve power, thermal, variability, timing, electromagnetics and reliability challenges across the spectrum of chip, package and system to promote first-time silicon and system success. ANSYS simulation and modeling tools offer you early power budgeting analysis for high-impact design decisions and foundry-certified accuracy needed for IC signoff.

System-aware IC power efficiency, power integrity and reliability

At the core of every electronics system is a chip that must meet multiple conflicting requirements, such as high performance, increased functionality, power efficiency, reliability and low cost. Ensuring the chip meets power efficiency, power integrity and reliability requirements as both a stand-alone component and within the electronics system calls for a system-aware chip design methodology. ANSYS uniquely offers a suite of multiscale, multiphysics solutions to support a chip-package-system (CPS) design flow.

The ANSYS semiconductor portfolio of power efficiency, power integrity and reliability solutions achieve ISO 26262 “Tool Confidence Level 1” (TCL1) certification. This certification enables automotive IC designers to meet rigorous safety requirements for ADAS and autonomous applications. Auto chip makers can leverage ANSYS PowerArtist, ANSYS Totem and ANSYS RedHawk family of multiphysics simulations for all ISO 26262 safety-related development projects at any Automotive Safety Integrity Level.

Foundry certified accuracy

With the cost of designing and implementing a system-on-chip (SoC) ranging from \$50 million to \$200 million, first-time working silicon is a must. IC designers require the most accurate simulation solution and consider foundry certification as the ultimate proof of accuracy. ANSYS semiconductor solutions have been certified by all leading foundries since 2006.

Production-proven solutions

Our software has enabled thousands of successful tape-outs across multiple technology nodes.

Applications

SOC POWER INTEGRITY

IP POWER & RELIABILITY

3D & 2.5D IC ANALYSIS

RTL POWER EFFICIENCY

SOC RELIABILITY

CHIP PACKAGE SYSTEM CO-DESIGN

SUBSTRATE NOISE

AUTOMOTIVE IC

7NM CHIP DESIGN







